REMARKS

Applicants respectfully request reconsideration of the present U.S. Patent application. Claims 13-16, 19, 20, 22-24 and 26-28 have been canceled. Claims 29-50 have been added. Because a number of claims have been added and cancelled during the prosecution of the present patent application, the ordering of the claims was no longer sequential. In some cases, Applicants have cancelled pending claims and added similar new claims so that the claims are sequentially ordered. Thus, claims 29-50 are pending.

REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 13, 14, and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,652,823 issued to Eto, et al. (*Eto*) in view of U.S. Patent No. 5,337,086 issued to Fujinami (*Fujinami*). Claims 13, 14, and 26 have been cancelled and, therefore, the rejection of claims 13, 14, and 26 is moot. Applicants will respond to the rejections of claims 14 and 26 as if new claims 29 and 41 have been rejected. For at least the reasons set forth below, Applicants submit that claims 29 and 41 are not rendered obvious in view of *Eto* and *Fujinami*.

The Manual of Patent Examining Procedure ("MPEP"), in § 706.02(j), states:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be both found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Thus, the MPEP and applicable case law require that a combination of references teach or suggest all of the claim limitations of rejected claims as well as provide motivation for the combination, to sustain an obviousness rejection under 35 U.S.C. § 103.

Claim 29 states:

> ...a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a **first order** determined by the write address generator...
>
> a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to **output pixel data in a second order, wherein the second order comprises a sub-block-by-sub-block row major order.**

(Emphasis added). Claim 36 similarly recites a "memory to store pixel data ... in a first order" and a "read address generator ... to ... cause the memory to output pixel data in sub-block-by-sub-block row major order." Claim 41 recites "storing pixel data in a memory in a first order" and "reading the pixel data out of the memory in a second order ... the second order comprises reading the pixel data sub-block-by-sub-block in row major order."

Regarding the recited elements of "a write address generator" and "a read address generator," the Office action directs the Applicants' attention to column 35, lines 13-30, wherein *Eto* states:

> ... **video data ... frames** are outputted through the switch 15. The output (see FIG. 15I) of the switch 15 is supplied to the memory 16, and temporarily stored in the memory 16 in response to the **write/read control signal** from the system controller 17. Then, the video data stored in the memory 16 is read out from the memory 16... in response the **write/read control signal** from the system controller 17...

Emphasis added. The Office action argues that the cited passages teach "a write address generator" and "a read address generator." The Applicants respectfully disagree.

The cited passage merely discloses using a write/read control signal to cause frames of video data to be outputted from a switch to a memory. Neither a "**write address generator**" nor a "**read address generator**" is discussed at all. In fact, Applicants can find nothing in the cited passage that discusses address generation. Therefore, Applicants find nothing in the cited

passage that discloses a "write address generator" or a "read address generator," as recited in claim 29.

The Office action states that *Eto* does not disclose causing the memory to output pixel data in a second order, wherein the second order comprises **sub-block-by-sub-lock in row major order**. Applicants respectfully agree with the Examiner that *Eto* does not disclose the recited element.

Regarding the recited element of causing "the memory to output pixel data in a second order, wherein the second order comprises a **sub-block-by-sub-lock in row major order**." the Office action directs the Applicants' attention column 4, lines 39-52, wherein *Fujinami* discloses:

> Now an explanation of calculator 2 will be given below with regard to the operation. The image data divided into macroblocks and further into subblocks as shown in FIG. 3 are stored in the frame memory 1 block by block. **The data of each subblock thus stored in the frame memory 1 is read out therefrom,** and then the difference between such data and the predictive image data outputted from the motion detector 9 is calculated by the calculator 2. Subsequently this difference data is inputted to the DCT circuit 3 where a discrete cosine transformation is executed. The data outputted from the DCT circuit 3 is supplied to the quantizer 4, and then the quantized data therefrom is supplied to the VLC circuit 5.

Emphasis added. The Office action argues that the cited passage teaches causing "the memory to output pixel data in a second order, wherein the second order comprises a sub-block-by-sub-lock in row major order." The Applicants respectfully disagree.

The cited passage merely discloses that "**each subblock thus stored in the frame memory 1 is read out therefrom,**" without any suggestion that the data is read out in row major order. Rows of pixels and **reading rows of pixels in row major order is not discussed at all.** Therefore, Applicants find nothing in the cited passage of *Fujinami* that discloses causing "the

memory to output pixel data in a second order, wherein the second order comprises a sub-block-by-sub-lock row major order," as recited in claim 29.

As shown above, neither *Eto* nor *Fujinami* teaches or suggests a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order as claimed by Applicants. Thus, no combination of *Eto* with *Fujinami* teaches or suggests a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Also, *Eto* fails to disclose "a write address generator" and "a read address generator" as recited by Applicants. For at least the above-stated reasons, Applicants respectfully submit that no combination of *Eto* with *Fujinami* renders claims 29, 36, and 41 obvious.

Dependent claims 15, 16, 27, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto* in view of *Fujinami*, and in further view of U.S. Patent No. 5,892,518 issued to Mizobata et. al. (*Mizobata*). Dependent claims 15, 16, 27, and 28 have been cancelled and, therefore, the rejection of claims 15, 16, 27, and 28 is moot. New claims 33, 34, 43, and 44 respectively recite the same limitations as claims 15, 16, 27, and 28. Claims 33 and 34 depend from claim 29. Claims 43 and 44 depend from claim 41. For at least the reasons set forth below, Applicants submit that new claims 33, 34, 43, and 44 are not rendered obvious by *Eto*, *Fujinami*, and *Mizobata*.

Mizobata is cited to teach "a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock and wherein processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the bounding are processed." Whether or not *Mizobata* discloses the limitations cited by the Office

action, it does not teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Thus, Applicants respectfully submit that no combination of *Eto*, *Fujinami*, and *Mizobata* renders claims 33, 34, 43, and 44 obvious.

Claims 20, 22, and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto*, in view of *Fujinami*, and in further view of U.S. Patent No. 6,208,350 B1 issued to Herrera (*Herrera*). Claims 20, 22, and 23 have been cancelled and, therefore, the rejection of claims 20, 22, and 23 is moot. Applicants will respond to the rejections of cancelled claims 20, 22, and 23 as if new claims 36, 38, and 39 respectively were rejected. For at least the reasons set forth below, Applicants submit that claims 36, 38, and 39 are not rendered obvious in view of *Eto*, *Fujinami*, and *Herrera*.

Claim 36 recites:

> a memory coupled to the command stream controller, the memory to store **pixel data** related to a macroblock in a **first order**, the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation...
>
> a read address generator coupled to the memory, the read address generator to cause the memory to **output the pixel data** related to a macroblock in a **second order**, the read address generator to cause the memory to output pixel data in **sub-block-by-sub-block in row major order**...

Thus, Applicants claim an apparatus that stores pixel data into a memory in a first order that is "based on output from an ... IDCT operation" and "a read address generator to cause the memory to output the pixel data in a second order" that is "sub-block-by-sub-block in row major order." As stated above, the MPEP and applicable case law require that a combination of references teach or suggest all of the claim limitations of rejected claims as well as provide motivation for the combination, to sustain an obviousness rejection under 35 U.S.C. § 103.

Herrera is cited as teaching "conventional texture mapping operations and bilinear filterings within motion compensation systems." Whether or not *Herrera* discloses the limitations cited by the Office action, it does not teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Thus, Applicants respectfully submit that no combination of *Eto*, *Fujinami*, and *Herrera* renders claim 36 obvious.

Applicants further submit that there is no suggestion or motivation to combine *Herrera* with *Eto*. MPEP § 2143.01 states:

> Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

The teaching or suggestion to make the claimed combination must be found in the prior art, not in Applicants' disclosure. *See In re Vaeck*, 20 USPQ2d 1438 (Fed. Cir. 1991). The Office action does not cite an explicit suggestion or motivation to combine *Herrera* with *Eto* and, therefore, if the suggestion exists, it must be implicit.

Eto discloses an apparatus that performs video encoding and video decoding. See, e.g., FIG. 1 and FIG. 7. *Herrera*, in contrast, discloses a combination of a modified graphics accelerator with software to create a cost effective hybrid solution to providing a personal computer with DVD capabilities. See, e.g., column 4, lines 63-66 and FIG. 8. *Herrera* states:

> The second type of solution, places the DVD processing task entirely on the PC's hardware ... providing such specialized circuitry **(e.g., a DVD decoder)** can be very expensive and result in significantly increased costs, which can be **devastating** in the highly competitive PC market. The specialized circuitry can also **reduce the performance of the PC** by requiring access to the PC's bus(es), interfaces and memory components, in some PC architectures.

See column 4, lines 37-46. *Herrera*, therefore, explicitly teaches away from *Eto*, rather than providing an implicit basis to combine the references. Because *Herrera* explicitly teaches away from *Eto*, Applicants respectfully submit that the combination of *Herrera* with *Eto* is improper.

Claims 38 and 39 depend from claim 36. For at least the reason that dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 38 and 39 are not rendered obvious by *Eto*, *Fujinami*, and *Herrera*.

Claim 24 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto*, in view of *Fujinami*, in view of *Herrera*, and in further view of U.S. Patent No. 5,446,495 issued to Tourtier,et al. (*Tourtier*). Claim 24 has been cancelled and, therefore, the rejection of claim 24 is moot. New claim 40 recites the same limitations as canceled claim 24. For at least the reasons set forth below, Applicants submit that new claim 40 is not rendered obvious in view of *Eto*, *Fujinami*, *Herrera*, and *Tourtier*.

Tourtier is cited as teaching "the particular motion compensation pipeline processings and multiple frame prediction operations" claimed by Applicants. Whether or not *Tourtier* discloses the limitations cited by the Office action, it does not teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Thus, Applicants respectfully submit that no combination of *Eto*, *Fujinami*, *Herrera*, and *Tourtier* renders claim 40 obvious.

Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto*, in view of *Fujinami*, and in further view of *Tourtier*. Claim 19 has been cancelled and, therefore, the rejection of claim 19 is moot. New claim 35 recites the same limitations as cancelled claim 19. For at least the reasons set forth below, Applicants submit that new claim 35 is not rendered obvious in view of *Eto*, *Fujinami*, and *Tourtier*.

As discussed above, whether or not *Tourtier* discloses the limitations cited by the Office action, it does not teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Thus, Applicants respectfully submit that no combination of *Eto*, *Fujinami*, and *Tourtier* renders claim 35 obvious.

CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, claims 29-50 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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MARKED VERSION OF THE AMENDED CLAIMS

29. (New) A circuit for generating motion compensated video, the circuit comprising:

a command stream controller to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output pixel data in a second order, wherein the second order comprises a sub-block-by-sub-block in row major order.

30. (New) The circuit of claim 29, wherein the processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame comprises processing circuitry to perform motion compensation operations and texture mapping operations utilizing common circuitry.

31. (New) The circuit of claim 29, wherein the first order corresponds to an output sequence of an inverse discrete cosine transform operation.

32. (New) The circuit of claim 29, wherein the first order is block by block in row major order.

33. (New) The circuit of claim 29, wherein the processing circuitry comprises a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock.

34. (New) The circuit of claim 29, wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed, and a second mode wherein all pixels within the bounding box are processed.

35. (New) The circuit of claim 29, wherein the circuit is pipelined.

36. (New) An apparatus comprising:

a command stream controller to manipulate motion compensation video data;

a memory coupled to the command stream controller, the memory to store pixel data related to a macroblock in a first order, the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation;

a read address generator coupled to the memory, the read address generator to cause the memory to output the pixel data related to a macroblock in a second order, the read address generator to cause the memory to output pixel data in sub-block-by-sub-block in row major order; and

a processing unit coupled to the read address generator and to the command stream controller, the processing unit to perform motion compensation operations and texture mapping operations utilizing common circuitry.

37. (New) The apparatus of claim 36, wherein the memory to store pixel data related to a macroblock in a first order comprises the memory to store pixel data related to a macroblock block by block in row major order.

38. (New) The apparatus of claim 36, wherein the processing unit further comprises:

a memory to store reference pixels;

a mapping address generator to provide read addresses for the reference pixels;

a bilinear filter coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels; and

a first-in-first-out (FIFO) buffer coupling the mapping address generator to the bilinear filter, the buffer to maintain sequence of the read addresses from the mapping address generator to the bilinear filter.

39. (New) The apparatus of claim 36, further comprising the read address generator coupled to a write address generator, the write address generator to generate synch points and the read address generator to receive the synch points to prevent the read address generator from overwriting valid data in the memory.

40. (New) The apparatus of claim 36, wherein the apparatus is pipelined.

41. (New) A method comprising:

storing pixel data in a memory in a first order based on output from an Inverse Discrete Cosine Transform (IDCT) operation;

receiving a command to generate a reconstructed video frame; and

reading the pixel data out of the memory in a second order, wherein the second order comprises reading the pixel data sub-block-by-sub-block in row major order.

42. (New) The method of claim 41, wherein storing pixel data in a memory in a first order based on output from an Inverse Discrete Cosine Transform (IDCT) operation comprises storing pixel data block by block in row major order.

43. (New) The method of claim 41, further comprising determining a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock.

44. (New) The method of claim 43, further comprising processing the pixel data in triangular regions, wherein in a first mode pixels inside a triangle within a bounding box are processed, and in a second mode all pixels within the bounding box are processed.

45. (New) A method of motion compensation of digital video data, the method comprising:

receiving a motion compensation command having associated correction data related to a macroblock;

storing the correction data in a memory block by block in row major order;

performing frame prediction operations in response to the motion compensation command;

reading the correction data from the memory sub-block by sub-block in row major order; and

combining the correction data with results from the frame prediction operations to generate an output video frame.

46. (New) The method of claim 45, wherein performing frame prediction operations further comprises:

generating a bounding box containing the macroblock; and

iterating the bounding the bounding box;

fetching reference pixels;

filtering the reference pixels;

averaging the filtered reference pixels, if necessary; and

adding correction data to the reference pixels.

47. (New) The method of claim 46, further comprising performing texturing operations for the macroblock.

48. (New) An article of manufacture comprising:

an electronically accessible medium providing instructions that, when executed by one or more processors, cause the one or more processors to

receive a motion compensation command having associated correction data related to a macroblock;

storing the correction data in a memory block by block in row major order;

perform frame prediction operations in response to the motion compensation command;

read the correction data from the memory sub-block by sub-block in row major order; and

combine the correction data with results from the frame prediction operations to generate an output video frame.

49. (New) The article of manufacture of claim 48, wherein the electronically accessible medium further comprises instructions that, when executed by one or more processors, cause the one or more processors to

generate a bounding box containing the macroblock; and

iterate the bounding the bounding box;

fetch reference pixels;

filter the reference pixels;

average the filtered reference pixels, if necessary; and

add correction data to the reference pixels.

50. (New) The article of manufacture of claim 49, wherein the electronically accessible medium further comprises instructions that, when executed by one or more processors, cause the one or more processors to perform texturing operations for the macroblock.